CLAIMS

What is claimed is:

1. A system comprising:

a processor;

a power supply coupled to the processor; and

a device coupled to the processor and the power supply and comprising:

an internal power supply bus configured to receive a power signal from the power supply; and

an isolation circuit configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal.

2. The system, as set forth in claim 1, wherein the system is a cellular phone.

3. The system, as set forth in claim 1, wherein the system is a personalized digital assistant (PDA).

4. The system, as set forth in claim 1, wherein the system is a handheld computer.

5. The system, as set forth in claim 1, wherein the device comprises a memory device.

6. The system, as set forth in claim 1, wherein the internal power supply bus is configured to provide the power signal to the device.

7. The system, as set forth in claim 1, wherein the isolation circuit is coupled between a pad on the device configured to receive the power signal and the internal power supply bus.

8. The system, as set forth in claim 1, comprising an input buffer comprising a control line configured to control the isolation circuit.

9. The system, as set forth in claim 8, wherein the isolation circuit comprises a p-channel field effect transistor (FET).

10. The system, as set forth in claim 9, wherein the gate of the p-channel FET is coupled to the control line of the input buffer.

11. The system, as set forth in claim 1, comprising an output buffer configured to buffer the device from the remainder of the system.

12. The system, as set forth in claim 11, comprising:

an input/output pad; and

circuitry coupled between the output buffer and the input/output pad and configured to tri-state the input/output pad.

13. A device comprising:

an internal power supply bus configured to receive a power signal; and

an isolation circuit configured to disconnect the internal power supply bus from the power signal.

14. The device, as set forth in claim 13, comprising a memory device.

15. The device, as set forth in claim 13, wherein the internal power supply bus is configured to provide the power signal to the memory device.

16. The device, as set forth in claim 13, wherein the isolation circuit is coupled between a pad on the memory device configured to receive the power signal and the internal power supply bus.

17. The device, as set forth in claim 13, comprising an input buffer comprising a control line configured to control the isolation circuit.

18. The device, as set forth in claim 17, wherein the isolation circuit comprises a p-channel field effect transistor (FET).

19. The device, as set forth in claim 18, wherein the gate of the p-channel FET is coupled to the control line of the input buffer.

20. The device, as set forth in claim 19, comprising an output buffer.

21. The device, as set forth in claim 13, comprising:

an input/output pad; and

circuitry coupled between the output buffer and the input/output pad and configured to tri-state the input/output pad.

22. A method of manufacturing a device for implementing a standby mode in a system comprising the acts of:

providing a device having a power bus configured to receive a power signal and to provide the power signal to a plurality of components in the device, wherein the power bus is internal with respect to the device;

providing an electrical path configured to deliver an external power signal to the internal power bus; and

providing an isolation circuit on the electrical path, the isolation circuit configured to disconnect the external power signal from the internal power bus.

23. The method of manufacturing a device for implementing a standby mode in a system, as set forth in claim 22, wherein the act of providing an isolation circuit comprises the act of providing a p-channel field effect transistor (FET).

24. The method of manufacturing a device for implementing a standby mode in a system, as set forth in claim 22, wherein the act of providing an isolation circuit comprises the act of providing an isolation circuit which is configured to disconnect the external power signal from the internal power bus in response to the occurrence of an event.

25. The method of manufacturing a device for implementing a standby mode in a system, as set forth in claim 24, comprising the act of providing an isolation circuit which is configured to disconnect the external power signal from the internal power bus in response to the occurrence of an event, and wherein the event comprises the expiration of a counter.

26. The method of manufacturing a device for implementing a standby mode in a system, as set forth in claim 25, wherein the act of providing an isolation circuit which is configured to disconnect the power signal from the internal power bus in response the occurrence of an event, and wherein the event comprises receiving a control signal at an input of the isolation circuit, and wherein the control signal is delivered in response to a

transitioning of the system from a normal mode of operation to a standby mode of operation.

27. The method of manufacturing a device for implementing a standby mode in a system, as set forth in claim 22, comprising providing one or more components, wherein the components are not coupled to the internal power bus.

28. The method of manufacturing a device for implementing a standby mode in a system, as set forth in claim 27, comprising providing an isolation circuit configured to disconnect the power signal from the internal power bus in response to the occurrence of an event without disconnecting the external power signal from the one or more components.

29. The method of manufacturing a device for implementing a standby mode in a system, as set forth in claim 22, comprising providing circuitry configured to drive an input/output pad into a tri-state condition.

30. A method of implementing a standby mode in a system comprising the acts of:

delivering a control signal to the input of an isolation circuit, the isolation circuit being coupled between a power supply and an internal power bus; and

isolating the power supply from the internal power bus by interrupting the path between the power supply and the internal power bus.

31. The method of implementing a standby mode in a system, as set forth in claim 30, wherein the internal power bus is configured to provide power to a memory device.

32. The method of implementing a standby mode in a system, as set forth in claim 30, wherein the act of delivering the control signal to the isolation circuit comprises the act of delivering the control signal to a p-channel field effect transistor (FET).

33. The method of implementing a standby mode in a system, as set forth in claim 30, wherein the act of isolating the power supply from the internal power bus occurs in response to the occurrence of an event.

34. The method of implementing a standby mode in a system, as set forth in claim 33, wherein the event comprises the expiration of a counter.

35. The method of implementing a standby mode in a system, as set forth in claim 30, comprising providing the power signal to the isolation circuit and to one or more components, wherein the components are not coupled to the internal power bus.

36. The method of implementing a standby mode in a system, as set forth in claim 31, wherein the isolation circuit is configured to disconnect the power signal from the internal power bus in response to the occurrence of an event without disconnecting the power signal from the one or more components.